



INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
MATERIALS MANAGEMENT DIVISION
Powai, Mumbai 400076.

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Detailed Technical Specifications for Mixed Signal ASIC Fabrication:

1. EP MPW/Mini@sic, H2 2022
2. Mini@sic, Area of 1875x1875 μm^2
3. UMC L65N Logic/Mixed Module/RF - LL/SP
4. On-silicon base area: 1 block(s)
5. Blocks containing-
 - I. Phase Locked loop
 - II. Programmable Current source
 - III. In memory computing
 - IV. Capacitive Front end
 - V. Energy Harvesting Circuit
6. Technology Size: 65nm
7. Die Numbers: 50
8. Packaging
 - I. In QFN 64 (9x9)
 - II. Number of packages: 20