

## INDIAN INSTITUTE OF TECHNOLOGY BOMBAY MATERIALS MANAGEMENT DIVISION Powai, Mumbai 400076.

## (PR No. 1000042876)

## (RFQ No.3600002887)

## **Technical Specification for Chip Fabrication**

| Sr.<br>no | Item Description  | Qty | Unit | Compliance<br>(Yes/No) | Additional info. if any |
|-----------|---|-----|------|------------------------|-------------------------|
| 1.        | Chip Fabrication<br>TSMC 65nm MS RF GP Shared<br>Block<br>Foundry: TSMC Technology:65nm<br>Flavor: MS RF GP Area:1 mm X 1.5<br>mm Sample Quantity: 100<br>Warranty: 1year | 1.5 | EA   |                        |                         |

|    | Quik- | Pak QFN100 Assembly                               | 1 | EA |  |
|----|-------|---|---|----|--|
|    |       | FN100-12MM-4MM)                                   |   |    |  |
| 2. | M1449 | ,<br>00   |   |    |  |
|    | 1.    | Packaging type: QFN                               |   |    |  |
|    | 2.    | Packaging body size: 12 mm                        |   |    |  |
|    |       | X 12mm  |   |    |  |
|    | 3.    | Package Lead count: 100                           |   |    |  |
|    | 4.    | Package Lead pitch: 0.4 mm                        |   |    |  |
|    |       | Package Assembly Qty:20                           |   |    |  |
|    | 6.    | Testing will be performed in                      |   |    |  |
|    |       | house in our lab. Since this is                   |   |    |  |
|    |       | a proprietary chip, we do not                     |   |    |  |
|    |       | want a third party to                             |   |    |  |
|    | _     | intervene in our testing.                         |   |    |  |
|    | 1.    | In-vitro test capability of the                   |   |    |  |
|    |       | chip along with electrical                        |   |    |  |
|    |       | FPGA based fast testing                           |   |    |  |
|    |       | (multi-channel simultaneous                       |   |    |  |
|    |       | testing) – will be done in-<br>house.             |   |    |  |
|    | 0     |   |   |    |  |
|    | 0.    | Physical verification (DRC, LVS, Antenna) will be |   |    |  |
|    |       | performed in-house in our                         |   |    |  |
|    |       | lab. Since this is a                              |   |    |  |
|    |       | proprietary chip, we do not                       |   |    |  |
|    |       | want a third party to                             |   |    |  |
|    |       | intervene in the physical                         |   |    |  |
|    |       | verification.                                     |   |    |  |
|    |       |   |   |    |  |