	INDIAN INSTITUTE OF TECHNOLOGY BOMBAY **MATERIALS MANAGEMENT DIVISION** **Powai, Mumbai 400076.**

PR No. 1000059359 **RFx No. 6100003226**

Technical Specification - Quantum Measurement Setup

NOTE

1. This procurement consists of four technically interdependent subsystems — Part A (**Digital to Analogue converter**), Part B (**Arbitrary Waveform Generator**), Part C (**QBox**), and Part D (**Cryogenic Filter**).
2. The four parts are being tendered together under a single tender to ensure technical compatibility. The compatibility between the four subsystems will form a key parameter in the evaluation of offers.
3. The four subsystems are required to function as a single integrated setup, and hence must be compatible with each other in terms of synchronization of applied voltage, demodulation of readout signals, connector compatibility, and device-level performance. Specifically,
    a. The **Digital-to-Analogue Converter** (DAC), **Qbox**, and **QFilter** must be compatible with each other to supply low-noise DC voltages to the gates and reservoirs of gate-defined quantum dot devices. When installed on the dilution refrigerator, the system shall allow an electron temperature of no more than 50 mK above the base temperature (~10 mK).
    b. The **Arbitrary Waveform Generator** (AWG) and the **Digital-to-Analogue Converter** (DAC) should be mutually compatible so that they can be used together to perform fast tuning of quantum dot devices through two-dimensional gate (charge stability) scans, with one gate voltage swept rapidly by the AWG and the other stepped by the DAC.
    c. The system should be controllable from a single software environment so that DAC voltage stepping and AWG sweeps are synchronized within one program.
4. A declaration on company letterhead regarding these compatibility requirements from the bidders for parts A, B, C, and D is mandatory at the time of bid submission. Please provide a declaration with technical details of the compatibility with the appropriate parts.
5. The technical evaluation will be based on individual technical specs as well as the compatibility between different parts
6. Prices for all four parts are to be clearly stated and specified separately in the quotation.
7. The financial L1 will be decided based on the combined price of all parts.

Part A: Digital to Analogue converter (DAC) – [Qty -2 Nos]

Sr. No.	Item Description	Detailed Technical Specification	Technical Compliance (Yes/No)	Additional Information (If any)
1	Number of independent channels	24		
2	Voltage	±10 V and ±2 V; should be able to configure for each channel separately		
3	DC Voltage resolution	24 bits or better		
4	Current output	10 mA or better		
5	Current sensing	Every channel should be able to measure the sourcing/leakage current independently with a Current resolution of 20 pA or lower		
6	Output impedance	50 Ohms		
7	Output filter	Selectable, with a minimum cut off of 10 Hz, and maximum cut off of 300 kHz for each output channel		
8	Voltage Stability	±2 µV		
9	Voltage noise floor	10 $nV/Hz^{1/2}$ or lower at 100 Hz		
10	Sample rate	1 MHz or better		
11	Rise time	5 µs or shorter		
12	Available waveforms on each channel	Sine, Square, Triangle.		
13	Output frequency	DC to 250 kHz or higher		
14	Waveform generator	One/channel		

15	Computer interfacing, Control and automation	Should have LAN and/Or USB interfaces. Should be able to control and automate using QCodes.		
16	Trigger options	Should have isolated trigger options for input and output		
17	Power requirements	Should operate on standard single-phase power outlets in India. Any power adapters required to operate the unit should be included.		
18	Formfactor	19-inch rack-mountable.		
19	Warranty	One-year warranty from the date of successful installation/commissioning of equipment.		

Part B: Arbitrary Waveform Generator – [Qty – 2 Nos]

Sr. No.	Item Description	Detailed Technical Specification	Technical Compliance (Yes/No)	Additional Information (If any)
1	No. of Output Channels	Shall have at least 20 independent output channels to provide arbitrary waveform, distributed in one 19-inch rack-mountable unit		
		All channels should be phase and time synchronous		
2	Output channel Characteristics	At least 16 channels (**Low Frequency Channels**), each capable of producing pulses in the frequency range of DC – 700 MHz or wider		
		At least 4 channels (**High Frequency Channels**), each capable of generating arbitrarily shaped microwave pulses to drive qubits or probe readout resonators with frequency in the range of 700 MHz to 10.5 GHz or wider. Signal generation		

		needs to be based on pure direct digital synthesis (DDS) technology for all frequencies up to 10.5GHz, without requiring any analog frequency upconversion stages (e.g., analog mixers).		
3	Low Frequency Output Channels Minimum Requirement	Digitizer sampling rate: 2 GSa/s for each channel or higher		
		DAC sampling rate: 2 GSa/s or higher		
		DAC Vertical resolution: 16-bit or higher		
		Number of Digital outputs: at least 1 per output channel or more.		
		Rise time < 500 ps at 0.8 Vpp (20%-80%)		
		Voltage range: 1 Vpp or wider.		
		Voltage noise: 10 nV/sqrt(Hz) at 100 kHz measured for 1 Vpp		
		Phase noise: -145 dBc/Hz or less (at 100M Hz with 10 kHz offset).		
		Total harmonic distortion: 65 dBc or higher		
		Spurious free dynamic range (SFDR): 55 dBc or higher (within the entire frequency range and without any external filtration).		
4	High Frequency Output Channels Minimum Requirement	Instantaneous Bandwidth: 800 MHz or wider.		
		DAC Vertical resolution: 16-bit or higher		
		Waveform sampling rate: minimum 2 GSa/s (1 GSa/s for each quadrature)		
		Allows to frequency multiplex tones within a span of at least 2GHz with no analog combiners and/or analog mixers.		
		Number of Digital outputs: at least 1 per output channel or more.		

		Full scale output power range from -11 to +16 dBm or wider.		
		Phase noise: -125 dBc/Hz at 6 GHz, 10 kHz offset or better		
		Total harmonic distortion: 40 dBc or higher at 0 dBm.		
		Spurious free dynamic range (SFDR) needs to be 75 dBc or higher at 0 dBm. The SFDR spec value must be specified for at least 1 GHz band around the carrier. SFDR spec value must be seamlessly attained, without any external filtering and with no calibration.		
		The integrated device must provide control of the absolute phase of the RF carrier for each output channel.		
5	Input Channels	The system should additionally have at least 4 input channels with the capability to demodulate and digitize measurement signals with carrier frequencies in the range 0 – 700 MHz or wider.		
6	Input Channels Minimum Requirement	Sampling rate: 2 GSa/s		
		ADC resolution: 12 bits		
		Input impedance: 50 Ω		
		Controllable gain: 32 dB		
7	Reference clock	The integrated device must have an input for an external frequency reference. It must support at least a standard 2 GHz clock.		
8	Power line	The instrument should be compatible with the standard Indian power line (supply)		
9	Markers	For sending marker and trigger signals, the integrated device must have at least one digital output channel per analog RF output.		

10	Operational Requirements	The integrated device must be capable of fully parametric waveform generation, waveform acquisition, real-time processing and control flow.		
		The integrated device must be able to output conditional execution of both microwave pulse and baseband pulse based on analog measurement outcome followed by signal demodulation and integration, with feedback latency ≤200		
		The integrated device must support the following operational latencies: Amplitude update < 16 ns, Phase update < 32 ns, Frequency update < 150 ns.		
		The integrated device must be capable of performing real-time analog feedback. The parameters of output pulses or continuous signals must be adjustable based on measured signals (or an arbitrary calculation performed on the input signals), without uploading an entirely new pulse waveform to the integrated device.		
		The integrated device must support real-time modulation of all pulse parameters including envelope, amplitude, phase, frequency, duration and offsets.		
		The integrated device must support real-time phase randomization for dynamical decoupling sequences.		
		The integrated device must support pre-processing of data (i.e. averaging) before sending it to the host PC.		
		The integrated device must support parallel and non-exclusive streaming of both the raw ADC traces and I, Q data.		
		The integrated device must allow the arbitrary control of sweep parameters utilizing FPGA -based (or equivalent)		

		control to perform parameter sweeps without time overhead, including parallel sweeping of multiple parameters.		
		The integrated device must allow extensive control flow, including if/else, for, while, switch statements, conditional plays, nested loops.		
		The integrated device must support programming new custom sequences, with access to fpga (or equivalent) logic, including conditional statements, without need to implement or understand low-level programming.		
		The integrated device must allow for adaptive automatic experiment termination based on arbitrary logic performed on running analysis results.		
		The integrated device must support running typical subroutines such as active qubit reset or mid-experiment frequency tracking on arbitrary sequences.		
		The integrated device must contain comprehensive library of hardware-optimized mathematical functions implementable on the FPGA (or equivalent), including multiplication, division, log, exp, sqrt, without the need of low-level programming		
		The integrated device must allow the ability to switch frequency and return by maintaining phase coherence.		
		The digital output channels must be synchronized with the analog outputs.		
		The integrated device must either be capable of calibration-free operation, or any required calibration of up- and down-conversion mixers for the high-frequency control in the integrated device and must be fully automatic and transparent to the user.		

		The integrated device must support real-time, dynamic updates to the running quantum sequence based on data received from the classical accelerator without requiring any pausing or recompilation of the program.		
11	Software & Control	Remote programming of each channel from a computer, via a single communication channel, which can be USB or Ethernet, should be provided		
		Must be compatible with QCodes		
		The integrated device must be controllable via pulse-level language compatible with Python API and with real-time processing. Comprehensive API documentation must be provided, including programming examples. The integrated device should be easy to install and program.		
		If the software or part of the software required to control the integrated device is not open source, the license must allow installing and using the control software on atleast 4 computers. It must not be tied to a single control computer.		
		Any future upgrade in the firmware should be provided free of cost		
12	Warranty	One-year warranty from the date of successful installation/commissioning of equipment.		

Part C: QBox (Breakout box) – [Qty – 2 Nos]

Sr. No.	Item Description	Detailed Technical Specification	Technical Compliance (Yes/No)	Additional Information (If any)
1	Connector interface	Fischer connector (both input and output), BNC connectors (input)		
2	Channel count	Minimum of 24 independent input signal channels per unit		
3	Shielding	Fully shielded metallic enclosure maintaining continuous electromagnetic shielding (Faraday cage) from the input to the output		
4	Control options	The breakout box should be able to connect 24 low-frequency channels to either a DAC channel, a ground, or leave them floating remotely, using commands sent from a computer.		
		The relays of the automated breakout box should be switchable within 100 ms.		
5	Electrical performance	(a) Low contact resistance and high insulation resistance between channels. (b) Minimal channel-to-channel crosstalk. (c) Suitable for precision DC and low-frequency measurements.		
6	Rack compatibility	19" rack-mountable		
7	Wiring	Low-noise wiring (e.g., twisted pairs) suitable for sensitive DC measurements		
8	Documentation	Complete pinout diagram and wiring documentation need to be provided		

Sr. No.	Item Description	Detailed Technical Specification	Technical Compliance (Yes/No)	Additional Information (If any)
9	Warranty	One-year warranty from the date of successful installation/commissioning of equipment.		

Part D: Cryogenic Filter (Qboard Accessories) – [Qty – 2 Nos]

Sr. No.	Item Description	Detailed Technical Specification	Technical Compliance (Yes/No)	Additional Information (If any)
1	Filter	At least 24 channels low pass filter with 2 stage RC and RF filters		
2	Filtering spec	a) 3 dB attenuation at 65 kHz b) At least 60 dB attenuation at 50 MHz		
3	Channel Isolation	More than 5 GOhm isolation per channel		
4	Connectors	Micro-D connectors for input and output		
5	Casing	Non-magnetic gold-plated copper		
6	Temperature Compatibility	Must be Compatible at cryogenic temperatures – mountable on the mixing chamber plate of a dilution refrigerator		
7	Magnetic field Compatibility	Compatible at high magnetic field – up to 9T		
8	Warranty	One-year warranty from the date of successful installation/commissioning of equipment.		